PATENT COOPERATION TREATY

PCT/JP2002/010161

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70) Rec'd PCT/PTO 23 JUN 2005

Applicant's or agent's file reference 310201239971	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)	
International application No. PCT/JP2002/010161	International filing date (day/month/year) 30 September 2002 (30.09.2002)	Priority date (day/month/year)	

International Patent Classification (IPC) or national classification and IPC
     G06F 9/30, 12/02, 12/06, 12/08, 12/10, 13/28

Applicant
RENESAS TECHNOLOGY CORP.

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of _____ 10 _____ sheets, including this cover sheet.

   ☐ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

      These annexes consist of a total of _____ sheets.

3. This report contains indications relating to the following items:

   I ☒ Basis of the report

   II ☐ Priority

   III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability

   IV ☐ Lack of unity of invention

   V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

   VI ☐ Certain documents cited

   VII ☐ Certain defects in the international application

   VIII ☐ Certain observations on the international application

Date of submission of the demand 30 September 2002 (30.09.2002)	Date of completion of this report 18 March 2004 (18.03.2004)
Name and mailing address of the IPEA/JP	Authorized officer
Facsimile No.	Telephone No.

Form PCT/IPEA/409 (cover sheet) (July 1998)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT	International application No.
	PCT/JP2002/010161

I. Basis of the report

1. With regard to the **elements** of the international application:*

☒ the international application as originally filed

☐ the description:

pages _____ , as originally filed

pages _____ , filed with the demand

pages _____ , filed with the letter of _____

☐ the claims:

pages _____ , as originally filed

pages _____ , as amended (together with any statement under Article 19

pages _____ , filed with the demand

pages _____ , filed with the letter of _____

☐ the drawings:

pages _____ , as originally filed

pages _____ , filed with the demand

pages _____ , filed with the letter of _____

☐ the sequence listing part of the description:

pages _____ , as originally filed

pages _____ , filed with the demand

pages _____ , filed with the letter of _____

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

☐ the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).

☐ the language of publication of the international application (under Rule 48.3(b)).

☐ the language of the translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/ or 55.3).

3. With regard to any **nucleotide and/or amino acid** sequence disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

☐ contained in the international application in written form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. ☐ The amendments have resulted in the cancellation of:

☐ the description, pages _____

☐ the claims, Nos. _____

☐ the drawings, sheets/fig _____

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

* *Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rule 70.16 and 70.17).*

** *Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

V. ` Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

	Claims		
Novelty (N)	Claims	1-20	YES
	Claims		NO
Inventive step (IS)	Claims	2, 12, 13, 19	YES
	Claims	1, 3-11, 14-18, 20	NO
Industrial applicability (IA)	Claims	1-20	YES
	Claims		NO

2. Citations and explanations

Document 1: Makoto ISHIKAWA et al., "Keitai Tanmatsu Kiki Muke My-con no Naizou Memory Tei-denryoku Shuhou," The Institute of Electronics, Information and Communication Engineers Gijutsu Kenkyu Hokoku, 18 July 2002, Vol. 102, No. 234, (ICD 2002 35-45), pages 1-6

Document 2: JP 2000-231550 A (Toshiba Corp.), 22 August 2000, abstract, column 12, lines 14-24, all drawings, (Family: none)

Document 3: JP 10-63502 A (Japan Science and Technology Corp.), 06 March 1998, entire text, all drawings, (Family: none)

Document 4: JP 4-195448 A (Hitachi, Ltd. et al.), 15 July 1992, page 3, upper right column, line 1 to lower left column, line 1 and page 6, lower right column, lines 6-14, and fig. 1, (Family: none)

Document 5: "SH7750 Programming Manual," Hitachi, Ltd., published in April 1998, pages 4/9, 10/128 and 10/130

Claim 1

Document 1 cited in the international search report
presents a "personal computer equipped with a CPU,
internal memory (XY memory or U memory) and a control
circuit (XYMC or UMC)."

In addition, document 2 cited in the international
search report discloses a "microprocessor equipped with
SPRAM that is used for specialized applications other than
cacheing, wherein the instructions for accessing the SPRAM
include instructions for transferring blocks into the
SPRAM and instructions for transferring blocks from the
SPRAM."

Furthermore, the technical concept wherein "address
specification fields for specifying the transfer source
address and the transfer destination address are provided
to the instructions for transferring data between sets of
memory" is well known, as disclosed in document 3 cited in
the international search report; therefore, the invention
that is set forth in claim 1 does not involve an inventive
step in the light of documents 1-3.

In the written response, the applicant asserts that
"either the source or the destination is specified in the
address specification field of an instruction in the
invention that is set forth in claim 1, whereas both the
source and the destination are specified in the address
specification field of an instruction in the invention
that is disclosed in document 3; therefore, the invention
that is set forth in claim 1 could not have been
configured simply by combining the inventions that are
disclosed in documents 1-3. The invention that is set
forth in claim 1 is characterized by the feature wherein
'when the address that is specified in the address
specification field of a specific request is an address
that has been mapped to the internal memory, said address
is set as either the transfer source address or the

transfer destination address for the block transfer,' and this technical characteristic is not disclosed or suggested in any of documents 1-3; therefore, the invention that is set forth in claim 1 involves an inventive step." However, the disclosure in claim 1 wherein "said specific instruction comprises an address specification field, and in cases when the address that is specified in the address specification field is an address that has been mapped to the aforementioned internal memory, said address is set as either the transfer source address or the transfer destination address for the aforementioned block transfer" cannot be considered to clearly indicate that the "specific instruction does not comprise an address specification field other than the address specification field that is set forth in claim 1 (i.e. that the specific instruction only comprises an address specification field that specifies either the transfer source address or the transfer destination address for the block transfer, and does not comprise a different address specification field for specifying the address from among the transfer source address or the transfer destination address for the block transfer that has not been specified." Therefore, it should be noted that there cannot be considered to be a significant difference between the "specific instruction" as set forth in claim 1 and the "instruction for transferring data between sets of memory, which comprises an address specification field for specifying the transfer source address and the transfer destination address," as disclosed in document 3.

Claim 2

The features that are set forth in claim 2 are not disclosed or suggested in any of documents 1-5 cited in the international search report.

Claims 3 and 4

The feature wherein the "CPU is provided with an accessible address register, and data transfers are conducted using the transfer source address data and the transfer destination address data that is provided in said address register," is well known, as disclosed in document 4; therefore, it would not be especially difficult for a person skilled in the art to configure the inventions that are set forth in claims 3 and 4 in the light of documents 1-4.

Claim 5

Document 1 indicates the "provision of a bus state controller that is connected to the control circuit (XYMC or UMC)." Therefore, the invention that is set forth in claim 5 does not involve an inventive step in the light of documents 1-4.

Claim 6

Document 1 indicates the "provision of cache memory, wherein the cache memory shares the CPU, the internal memory (XY memory or U memory), the control circuit (XYMC or UMC) and the logic bus." Therefore, the invention that is set forth in claim 6 does not involve an inventive step in the light of documents 1-3.

Claim 7

Document 1 indicates that the "internal memory (XY memory or U memory) is allocated in one portion of the non-cache space." Therefore, the invention that is set forth in claim 7 does not involve an inventive step in the light of documents 1-3.

Claim 8

Document 1 indicates the "provision of dedicated buses (an X bus and a Y bus) that are connected to the control circuit (XYMC) and the internal memory (XY memory)." Therefore, the invention that is set forth in claim 8 does not involve an inventive step in the light of documents 1-3.

Claim 9

Document 1 indicates the "provision of a cache controller (CCN)," and the "CCN and XYMC" that are indicated in document 1 are considered to correspond to the "control circuit" that is set forth in claim 9; therefore, the invention that is set forth in claim 9 does not involve an inventive step in the light of documents 1-3.

Claim 10

Document 5 (pages 4/9 and 10/130) indicates a "pre-fetch instruction (an operating instruction for the first cache memory)." Therefore, the invention that is set forth in claim 10 does not involve an inventive step in the light of documents 1-3 and 5.

Claim 11

Document 5 (page 10/128) indicates a "write-back instruction (an operating instruction for the second cache memory)." Therefore, the invention that is set forth in claim 11 does not involve an inventive step in the light of documents 1-3 and 5.

Claims 12 and 13

The features that are set forth in claims 12 and 13 are not disclosed or suggested in any of documents 1-5.

Claim 14

Document 1 indicates the "provision of a DMAC that is connected to the bus state controller" (for example, refer to fig. 1); therefore, the invention that is set forth in claim 14 does not involve an inventive step in the light of documents 1-4.

Claim 15

Document 1 indicates that "each of the sets of external memory are connected to via the bus state controller," and thus, in essence, is considered to comprise a means that corresponds to the "external interface circuit" that is set forth in claim 15; therefore, the invention that is set forth in claim 15 does not involve an inventive step in the light of documents 1-4.

Claim 16

Document 1 presents a "personal computer wherein the CPU, the cache memory, the internal memory that is not cached into the cache memory (XY memory or U memory) and the control circuit (XYMC or UMC) are connected to the logic bus."

In addition, document 2 discloses a "microprocessor equipped with SPRAM that is used for specialized applications other than cacheing, wherein the instructions for accessing the SPRAM include instructions for transferring blocks into the SPRAM and instructions for transferring blocks from the SPRAM."

Furthermore, the technical concept wherein "address specification fields for specifying the transfer source address and the transfer destination address are provided to the instructions for transferring data between sets of memory" is well known, as disclosed in document 3 cited in the international search report; therefore, the invention

that is set forth in claim 16 does not involve an inventive step in the light of documents 1-3.

In relation thereto, refer again to the items indicated in relation to claim 1 (the opinion pertaining to the assertions by the applicant in the written response).

Claim 17

Document 1 indicates the "provision of dedicated buses (an X bus and a Y bus) that are connected to the control circuit (XYMC) and the internal memory (XY memory)." Therefore, the invention that is set forth in claim 17 does not involve an inventive step in the light of documents 1-3.

Claim 18

Document 5 indicates a "pre-fetch instruction (an operating instruction for the first cache memory)" and a "write-back instruction (an operating instruction for the second cache memory)." Therefore, the invention that is set forth in claim 18 does not involve an inventive step in the light of documents 1-3 and 5.

Claim 19

The features that are set forth in claim 19 are not disclosed or suggested in any of documents 1-5.

Claim 20

Document 1 presents a "personal computer equipped with a CPU, a bus, internal memory (XY memory or U memory), a control circuit (XYMC or UMC) and a bus state controller."

In addition, document 2 cited in the international search report discloses a "microprocessor equipped with SPRAM that is used for specialized applications other than

cacheing, wherein the instructions for accessing the SPRAM include instructions for transferring blocks into the SPRAM and instructions for transferring blocks from the SPRAM."

Furthermore, the technical concept wherein "address specification fields for specifying the transfer source address and the transfer destination address are provided to the instructions for transferring data between sets of memory" is well known, as disclosed in document 3 cited in the international search report; therefore, the invention that is set forth in claim 20 does not involve an inventive step in the light of documents 1-3.

In relation thereto, refer again to the items indicated in relation to claim 1 (the opinion pertaining to the assertions by the applicant in the written response).